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Systematic design of hybrid high power microwave amplifiers using large gate periphery GaN HEMTs

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ABSTRACT

In this paper, a design methodology for realization of hybrid microwave power amplifiers (PAs) using discrete GaN HEMTs is systematically explained. High power solid-state amplifiers usually suffer from self-heating, high frequency instability, unbalanced feeding effects and suchlike that should be carefully taken into account in a reliable and robust design. Though most of these issues are discussed in some of the previously published literatures, a single self-contained document that systematically describes the hybrid microwave PA design is limited. In this work, a comprehensive design methodology for implementation of high frequency PA is presented while the important challenges of high power amplifier design are discussed in more detail and several useful practical hints are given. Especially, we focus on hybrid PAs that are realized using large gate periphery GaN HEMTs. As a real example, a PA is fabricated using a 0.25 μm GaN on SiC HEMT transistor with a gate width of 12.5 mm. The fabricated PA achieves a 12 dB small-signal gain, 30 W output power, and 52% PAE across the frequency range of 9–9.8 GHz. The thermal analyses of the power transistor are performed using a 3D model, which is developed in ANSYS software and calibrated by measured data. The model can be used to calculate the transistor channel temperature and consequently predict the device lifetime.

1. Introduction

High power amplifiers (HPAs) are major building blocks of high frequency transmitters. Vacuum tube PAs have been widely used in different high power and high frequency applications. They can provide high output power but they are heavy and occupy a relatively large area. In addition, they need high DC voltage in range of kV while suffering from short lifetimes and low power added efficiencies (PAEs). Recently, high power solid-state amplifiers have emerged as a promising candidate for realization of high frequency PAs, due to their unique characteristics. They can provide good properties such as higher power density, sufficient efficiency, smaller size, convenient reliability and appropriate lifetime [1]. Some possible applications are satellite communication, wireless base station and high frequency radars [2–4].

Different technologies have been used for realization of high frequency power amplifiers (PAs) [5–10]. Monolithic microwave integrated circuits (MMICs) provide compact size, excellent repeatability and adequate bandwidth [5], but they need sophisticated and expensive manufacturing process and they are not very suitable for high power applications [6]. Quasi-monolithic integrated technology (QMIT) can exhibit proper frequency response and thermal behavior, but it needs thin-film technologies for realization [7,8]. Hybrid integration technique is also an appropriate method for realization of HPAs. Hybrid PAs can easily be realized using discrete elements which are made from different materials. Furthermore, they can be fabricated on inexpensive substrate with an appropriate thermal characteristic [1,9]. However, the interconnect parasitics can deteriorate the RF frequency response at few tens of GHz [10] and limit the PA bandwidth.

High frequency PA should meet several stringent requirements such as sufficient output power, wide bandwidth, high PAE, small size, appropriate linearity and proper stability. In the recent years, many technical issues in design and realization of solid-state HPAs have been solved and documented [9,11–16]. Therefore, it would be very useful to gather all these accumulated information and structure them in a single article.

In this paper, a comprehensive design methodology for realization of hybrid microwave HPAs is systematically explained and their high frequency design considerations, thermal and reliability concerns and stability issues are discussed in more details. As a real example, a HPA is fabricated using multi-finger TGF2023-2-10 GaN on SiC HEMT. It provides a 12 dB small-signal gain, 52% PAE and 30 W output power in the frequency range of 9–9.8 GHz. The paper is organized as follows. In the next section, the proposed systematic design procedure for realization of high frequency HPAs is explained and different challenges of

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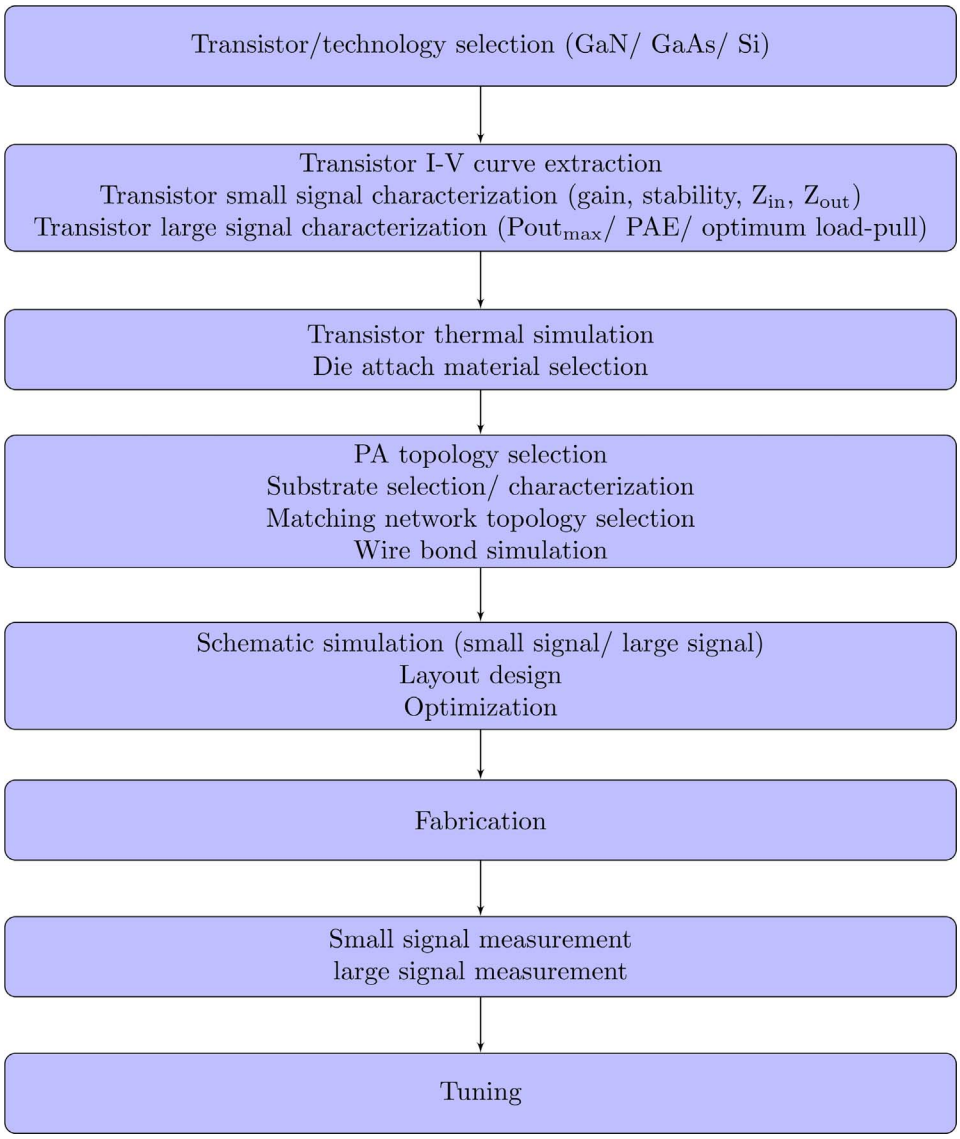


Fig. 1. The proposed flow-graph for design of high frequency PAs.

HPA design and the proper solutions to them are well covered. The proposed circuit simulation and measurement results are described in Section 3. Finally, a summary of the important results and conclusions has been derived in Section 4.

2. Design methodology

Realization of high frequency HPA is a challenging task due to many restrictions in material selection, characterization facilities, design specifications, and fabrication capabilities. Therefore, selecting an appropriate well-structured systematic design approach is vital for a first-time successful implementation. The flow graph of a proposed design procedure is shown in Fig. 1. It consists of technology/transistor selection, high frequency characterization of active and passive elements, transistor thermal characterization, matching network design, optimization, package simulation, fabrication, measurement and final tuning. These steps are described in the following sub-sections in details.

2.1. Transistor/technology selection

Selecting an appropriate transistor is a major step in the PA design procedure. The transistor should provide high gain, sufficient output power, appropriate PAE, and low thermal resistance. A HPA is implemented either by combing some identical low power transistors or by using a high power transistor with a large gate width. Combined PAs can handle high output power and show appropriate thermal performance, as thermal sources are separated, however, they usually suffer from phase mismatch, which effectively lowers their power gains and PAEs [1]. In addition, they can potentially become unstable, due to the odd mode oscillation [17]. Large gate periphery devices provide higher gain, smaller size, and more stable characteristic, but the reliability is a concern for them [18] and also they suffer from low frequency instability, self-heating, and unbalanced feeding effect [19]. Furthermore, the input and output impedance of large gate devices are very small, and thus their wideband impedance matching is more critical [9].

In comparison with GaAs and Si devices, GaN transistors provide higher breakdown voltage, lower thermal resistance, higher power density, and smaller size [20]. Therefore, they are a good choice for realization of high power amplifiers. In this work, TGF2023-2-10, a 0.25 μm GaN on SiC HEMT with 80 gate fingers, is selected for implementation of the proposed sample X-band HPA. The transistor f_T is about 20 GHz while it is unconditionally stable in the X-band. The maximum power density is about 3.5 W/mm (3.5 W per mm gate width) and the breakdown voltage is 100 V. The saturated output power is about 35 W at 10 GHz where the corresponding large-signal gain is 9 dB and its measured thermal resistance is 3.24 °C/W.

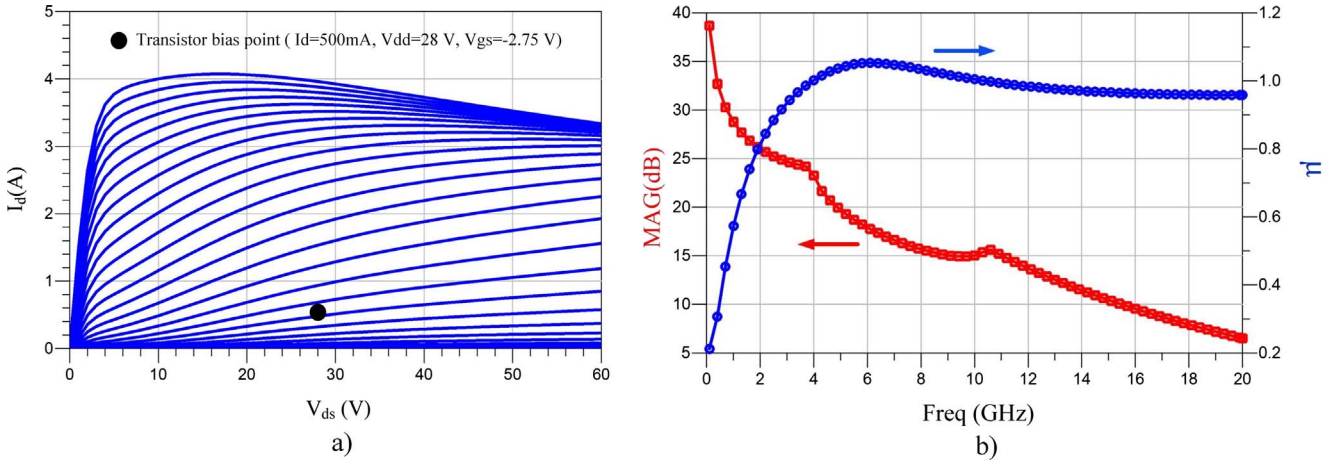


Fig. 2. (a) The I-V curve of the transistor under pulse mode condition with duty cycle of 10% and PRF of 10 kHz. (b) The maximum available gain (MAG) and stability factor of the transistor at V_{dd} = 28 V and I_d = 500 mA.

2.2. Characterization of the RF transistor

Successful implementation of high frequency PA requires precise characterization of the transistor in term of I-V curve, thermal characteristic and nonlinear parasitic extraction. The TGF2023-2-10 I-V curve is shown in Fig. 2a. It is measured under pulse mode condition with duty cycle of 10% and pulse repetition frequency of 10 kHz. As shown, the transistor pinch-off voltage, knee voltage and the maximum drain current are −3 V, 6 V and 4 A, respectively. The transistor bias point is V_{dd} = 28 V, V_{gs} = −2.75 V and I_d = 500 mA, which can provide an appropriate transistor transconductance. In order to determine the transistor high frequency instability region, the transistor S-parameters are measured at this bias condition, see Fig.2b. The transistor maximum available gain (MAG) at 9 GHz is about 15 dB while the transistor is unconditionally stable from 4 GHz to 10 GHz.

Though the small-signal model can predict the transistor linear behavior, it does not give sufficient information required for high frequency PA design. Under large-signal conditions, the device parameters have large variations, which should be taken into account. Therefore, employing an appropriate large-signal model is vital for a reliable PA design. A simple large- signal model of TGF2023-2-10 is shown in Fig. 3a. The model is derived from the conventional π model of the transistor, in which the C_{gd} capacitor is removed and its Miller effects are added to C_{gs} and C_{ds} and shown as C_{in} and C_{out}. This model also has been already used in [21,22] to improve the PA efficiency by shaping the gate and drain voltages of the transistor, based on the extracted transistor nonlinear capacitors. The L_{wire} and R_{wire} are equivalent inductance and resistance of the drain and gate wire bonds. They are extracted by simulating the proposed wire bond structures of drain and gate pads in HFSS simulator. The values of L_G, R_G, L_D, R_D, L_S and R_S, the transistor pad parasitic elements, are available in transistor datasheet [23]. Since C_{in}, C_{out} and g_m are the major sources of transistor nonlinearity, they must be modeled precisely. The nonlinear characteristics of these elements are shown in Figs. 3b, c and d. The C_{in} and C_{out} are obtained by measuring the transistor S-parameters for different gate-source and drain-source voltages and de-embedding the wire bonds and transistor pad parasitic effects. This approach provides a good insight into the nonlinear behavior of the transistor parasitic elements.

In PA design procedure, source-pull and load-pull analyses should be carried out in order to find the optimal input and output terminations. This necessitates an accurate nonlinear transistor model. The proposed PA is designed using an available commercial nonlinear TGF2023-2-10 model (provided by Modelithics Inc.) [23], in which all the transistor parasitic elements are extracted up to 40 GHz for different temperatures and bias conditions. It can be used for both continuous and pulse mode simulations while it precisely models the self-heating effect.

The optimal output termination can be selected for either power tuned or efficiency tuned strategy. The simulated load-pull of the transistor is shown in Fig. 4. Simulation results show that the maximum P_{out} and the maximum PAE are achieved at $Z_{L1} = Z_0 * (0.043 + j0.073)$ and $Z_{L1} = Z_0 * (0.039 + j0.096)$, respectively, with the source impedances of $Z_{s1} = 0.55 + 0.3j$ and $Z_{s2} = 5$. The maximum output power and PAE are 45.7 dBm and 52%, respectively. As it is shown, the optimum input impedance is very small and thus the wideband impedance matching cannot easily be obtained.

2.3. Thermal simulation

Since GaN on SiC HEMT exhibits a high power density, its proper thermal design is necessary. A good thermal management can effectively improve the power gain, output power and reliability of the PA. In addition, by using an accurate thermal model, the transistor maximum channel temperature can be obtained and consequently the lifetime of the device can be predicted. A 3D thermal model of the power transistor is developed in ANSYS software. Drain current of the transistor with gate width of 80 * 125 μm is about 500 mA. This means a 6.25 mA drain current and 175 mW power dissipation for each transistor finger at drain voltage of 28 V. In the proposed thermal model, the gates areas are considered as the heat sources and the heat-sink is considered as a perfect thermal conductor at a fixed temperature of 85 °C. As shown in Fig. 5, the maximum channel temperature is about 143.4 °C. The simulated thermal resistance of transistor is about 4.17 °C/W which has a good consistency with the measured data in [24]. The transistor channel temperature and its median-life for different conditions are extracted based on the proposed thermal model and the channel temperature-median lifetime curve provided by the manufacturer [24], see Table 1. As shown, the pulsed biasing method reduces the self-heating problem and thus improves the PA characteristic effectively.

In HPA design, the channel heat should be transferred to the surrounding environment with the lowest possible thermal resistance. Therefore, thermal property of the transistor substrate, die-attach and carrier materials have an important role in the thermal behavior of the PA. Since, the SiC substrate of TGF2023-2-10 has a high thermal conductivity (about 430 W/m·°C) [25], the thermal conductivity and thickness of the die-attach material interposed between the substrate and the carrier, play a vital role in heat spreading. Furthermore, the uniformity of die-attach materials can strongly affect the thermal behavior and life-time of the transistor. This is investigated in [26], in

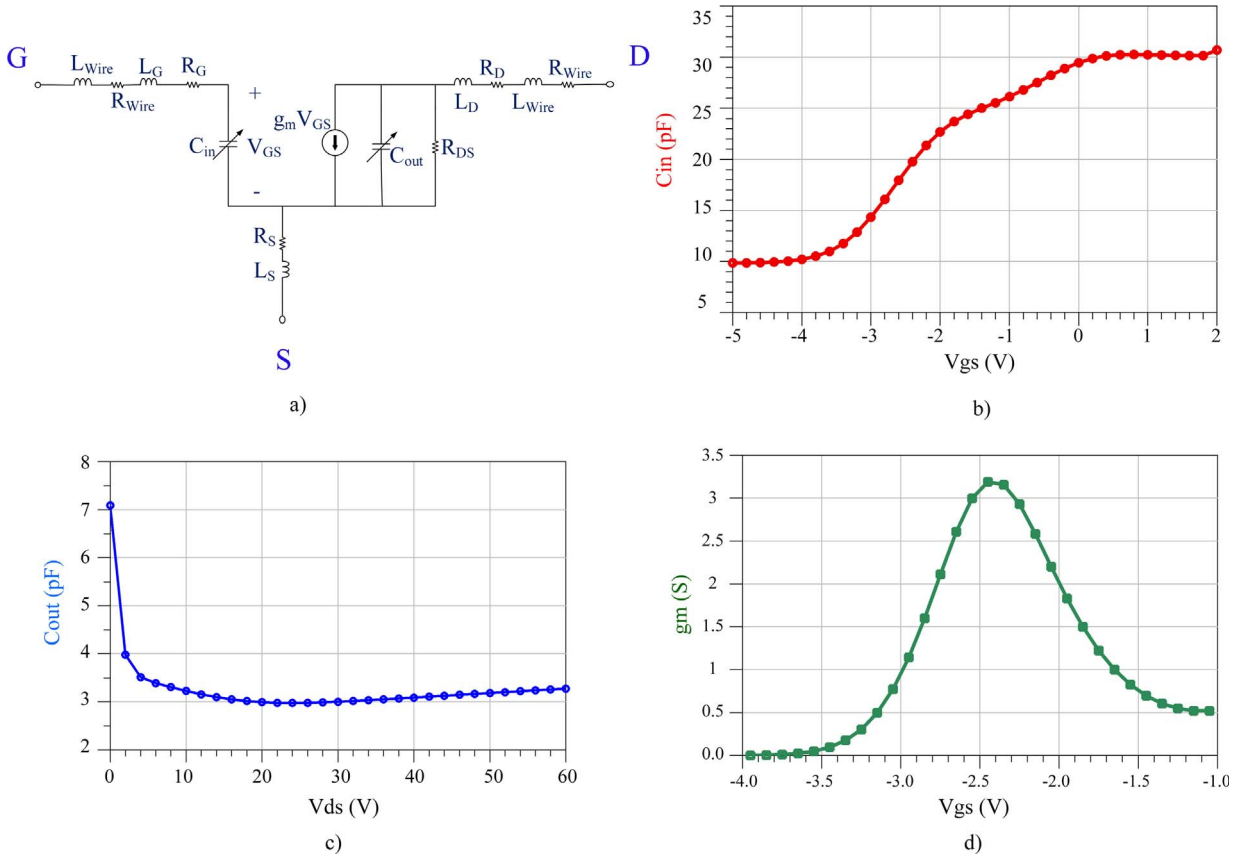


Fig. 3. (a) A simple large signal model of the transistor. (b) Nonlinear C_{in} of TGF2023-2-10 versus gate-source voltage. (c) Nonlinear C_{out} of TGF2023-2-10 versus drain-source voltage. (d) Nonlinear transconductance of TGF2023-2-10 versus gate-source voltage.

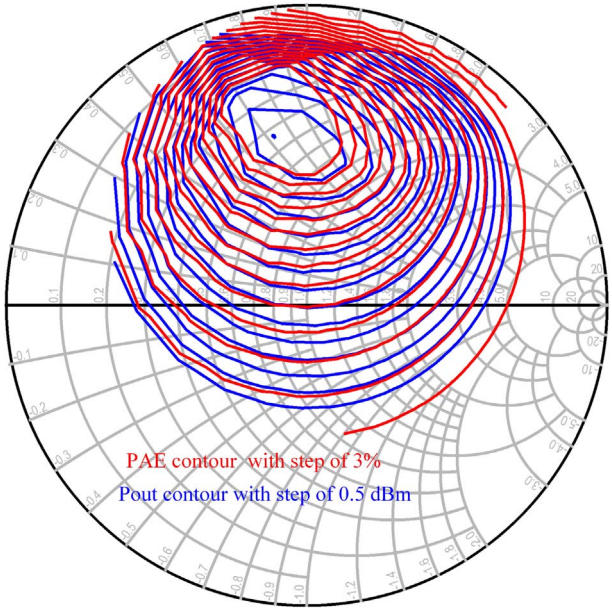


Fig. 4. The simulated PAE and Pout contour of the selected transistor.

which the non-uniformity was simulated by incorporating air bubbles with different sizes into the die-attach material. The Au80/Sn20 die-attach material provides a sufficient uniformity, proper thermal conductivity, and controllable thickness. In addition, it has a good compatibility with the gold plated backside transistors. Therefore, it is an excellent choice for fixing the high power GaN HEMT to the carrier.

The influence of different die-attach materials on a PA performance

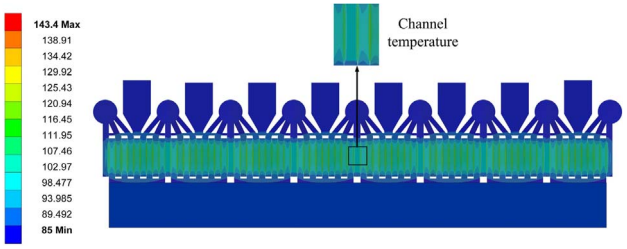


Fig. 5. Temperature distribution in °C obtained from a 3D thermal simulation of TGF2023-2-10 at drain current of 500 mA and drain voltage of 28 V ($P_{dissipation}$ = 14 W) in CW mode. The base-plate temperature is set to 85 °C.

Table 1
The transistor channel temperature and the corresponding median-life at different conditions.

Condition	Transistor channel temperature (°C)	Device median life-time (h)
$P_{dissipation}$ = 14 W, CW	143.4	3e9
$P_{dissipation}$ = 36 W, CW	235	8e5
$P_{dissipation}$ = 36 W, duty cycle = 10%, pulse width = 20 μs	169	2e8
$P_{dissipation}$ = 36 W, duty cycle = 20%, pulse width = 20 μs	178	9e7

are experimentally investigated and presented in Fig. 6. Three identical PAs are fabricated using die-attach materials Elcolit 323 (with thermal conductivity of 3.5 W/m·°C), Sk70N (with thermal conductivity of 50 W/m·°C), and Au80/Sn20 preform (with thermal conductivity of

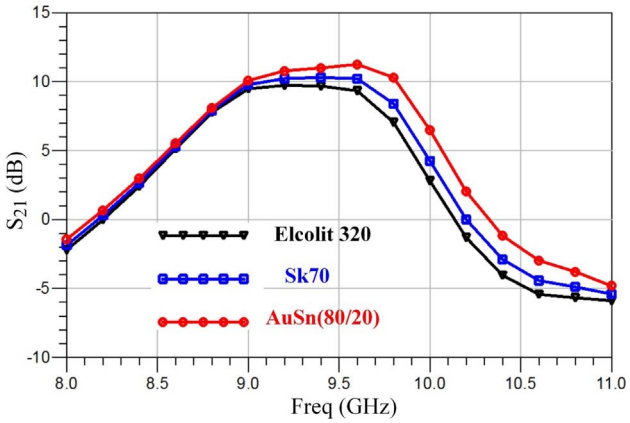


Fig. 6. The power gain of three identical PAs fabricated using die-attaches of Elcolit 320, Sk70 and AuSn (80/20).

57 W/m·°C). As shown in Fig. 6, the PA employing the Au80/Sn20 die-attach provides the best thermal performance and consequently gives the maximum power gain.

The transistor carrier should have a high thermal conductivity and a thermal expansion coefficient similar to that of SiC substrate. In such conditions, the transistor channel heat is removed effectively while minimum thermomechanical stress is induced in the structure. Lower channel temperature and thermomechanical stress guarantee a longer lifetime for the device. Although Cu/Mo and Cu/W provide lower thermal coefficients in comparison with Cu, however Cu exhibits a much higher thermal conductivity. Thus, we preferred gold plated Cu carrier and heat sink in our PA.

2.4. Hybrid high power amplifier design

The class of PA should be chosen based on the required bandwidth, linearity and PAE. Harmonic tuned PAs such as Class-F and inverse Class-F usually provide sufficient PAE, but they suffer from relatively limited bandwidths and nonlinear performances[27,28]. Furthermore, they need appropriate matching networks at higher harmonic frequencies, which is very difficult to be obtained at X-band frequencies due to the large parasitic elements of the high power transistor. The switching power amplifiers such as Class-E and Class-D exhibit high efficiency; however, they cannot easily be realized at X-band frequencies [29]. Reduced conduction angle PAs [30] such as Class-C PAs also provide high efficiency but they suffer from a low output power and a worse linearity performance. Class-AB PA is a conventional class for implementation of high frequency PAs, which can provide sufficient bandwidth, appropriate PAE, and convenient linearity [31]. Class-J will also provide a wider bandwidth [32], however it requires the second harmonic matching, which is hard to obtain for large periphery gate devices at X-band frequencies. The proposed PA is biased at deep Class-AB, V_{dd} = 28 V and I_{dQ} = 500 mA (0.125 I_{max}), which provides the maximum transistor transconductance.

High power transistors usually exhibit relatively large parasitic elements that limit the PA bandwidth. Furthermore, in the hybrid configuration, the wire bond interconnects exhibit extra parasitic inductances that further deteriorate the PA frequency response. Therefore, design of a wideband hybrid HPA is a challenging task. In the proposed hybrid PA, an acceptable bandwidth is achieved by appropriate selection of substrate, wire bond structure and matching networks topology. Selecting an appropriate substrate can affect the PA characteristics in terms of size, bandwidth and thermal behavior. Using a high dielectric constant substrate reduces the sizes of the matching networks and improves the PA bandwidth. However, high dielectric constant substrates usually suffer from relatively higher insertion loss [9] which can lower the PA power gain. Using a substrate with a better thermal conductivity improves the device heat transfer and consequently increases its median lifetime. Therefore, high thermal conductivity substrates such as alumina substrates are commonly used in fabrication of high power amplifiers.

In order to achieve a wide bandwidth characteristic, the discontinuity between input/output impedance of the transistor and impedance of the bonding pad on the matching network should be minimized [9]. Due to the relatively low input/output impedances of TGF2023-2-10 transistor at the desired frequency band (X-band), a high dielectric constant substrate with a low dielectric thickness (Rogers RO3010 with ϵ_r = 11.2 and H = 10 mil) is chosen for realization of the matching network. This effectively reduces the impedance discontinuity and thus improves the PA bandwidth. The PCB dielectric constant, given by the manufacturer, is usually an average value of measured ϵ_r for different PCB sheets. Therefore, the real ϵ_r of the utilized PCB can slightly differ from that of given in the data sheet. In order to have a reliable design, the dielectric constant of the substrate should be carefully measured using an appropriate test structure and then the high frequency simulations must be calibrated based on this measured ϵ_r. The high frequency ϵ_r of 11 is obtained for the PCB Rogers RO3010 at frequency of 9 GHz based on our high frequency measurements.

Since a HPA usually consumes relatively high power, the DC current and power handling capability of the transmission lines should be checked. Otherwise, especially at continuous wave (CW) mode, the electro-migration mechanism can destroy the interconnects. In the proposed sample PA, the maximum DC current is about 1.5 A. The simulation results using Saturn PCB toolkit show that a minimum width of 300 μm for transmission line on our selected substrate is needed to conduct such a DC current. In our design to assure no electro-migration failure and provide a good power handling capability, the minimum width of the transmission line is set to 900 μm.

Radial stub matching technique provides a rather wideband characteristic [15]. Therefore, it is used in realization of our input and output matching networks. The number of radial stub, width and length of the transmission lines are optimized for the best performance using random and gradient optimization strategies that is provided in commercial circuit design software like ADS (advanced design systems).

The wire bonds length and the wire bonds structure can also affect the PA characteristic strongly. Therefore, it is necessary to design them precisely using an accurate 3D full-wave simulator like HFSS or CST studio. Drain pads of the high power transistors are usually bonded with a large number of wire bonds to improve its power handling capability. TGF2023-2-10 transistor has 8 gate pads and one drain pad. In order to reduce the parasitic inductance, the wire bonds length should be minimized. Therefore, an appropriate carrier structure is designed to place the transistor at the same height of the matching networks in order to decrease the wire bonds length, see Fig. 7. In the proposed circuit, the gate pads and the drain pad are bonded to the matching networks using two and eight gold wire bonds with diameter of 25 μm, respectively. Parallel wire bonds reduce the equivalent inductance and improves the PA bandwidth. Reliable circuit design requires accurate values of the wire bond parasitic elements. In order to extract the

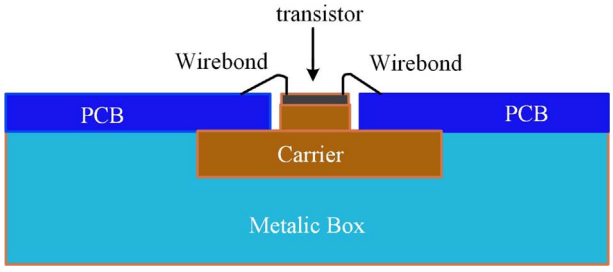


Fig. 7. Schematic cross sectional view of an assembled transistor in hybrid technology.

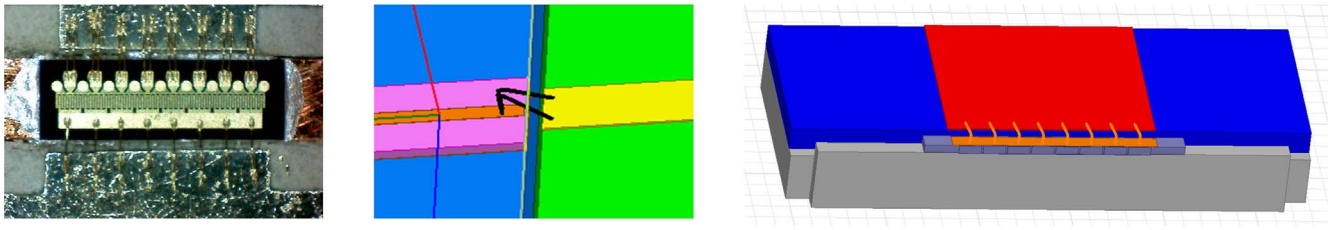


Fig. 8. The wire bonds: (a) Implementation. (b) 3D model of gate wire bonds in HFSS simulator. (c) 3D model of drain wire bonds in HFSS simulator.

parasitic elements, the wire bond structures in the gate (Fig. 8b) and drain (Fig. 8c) are modeled and excited using wave ports in HFSS simulator and their high frequency models are extracted up to 20 GHz. Wire bonds length is approximately 300 μm and the spaces between them at the gate and drain are 60 μm and 300 μm, respectively.

2.5. High frequency simulation

Accurate analysis of hybrid X-band matching networks needs 3D full-wave electromagnetic (EM) simulations that are complexed and very time consuming. Therefore, we suggest using a faster and simpler EM simulation, e.g. 2.5D EM simulator of Momentum available in ADS, in order to evaluate different matching network topologies and select the best structure. Then, at the end, check the selected structure only using an appropriate 3D EM simulator with sufficient mesh density.

Another important task in design of high power amplifier is stability analysis. Especially if large gate periphery devices are used, different mechanisms may cause oscillation of PA. Parameter of μ greater than 1 guarantees that the PA is unconditionally stable [33]. The transistor in this work is potentially unstable at frequencies lower than 4 GHz, see Fig. 2b. In order to prevent this low frequency oscillation, a series resistor is placed in the gate bias path to suppress the low frequency gain and thus improve the PA stability. As shown in Fig. 9, the stability resistor effectively improves the PA stability while it does not deteriorate the high frequency gain of the PA.

Large gate power transistor usually oscillates in the frequency range of 10 Hz to 50 MHz. This instability, which cannot be predicted by the stability analysis, is mainly due to the defects that exist in the transistor structure. However, this issue can easily be handled by using a large bypass capacitor and a series inductor in the bias network as described in [17].

In high power amplifiers, usually multiple transistors are used in parallel configurations. Although this is not the case in our fabricated sample circuit, it worth noting that any variation in any parameter of these transistors (e.g. g_m or $V_{pinch-off}$) or any imbalance in input/output impedances seen by these transistors causes mismatches in the configuration, which can lead to odd-mode oscillations due to the finite isolation of the transistors. In order to prevent happening of this issue, all transistors should be well-matched and all drain and gate pads must be connected to the matching network with the shortest possible line and bond wires. In addition, to enhance the isolation among the transistors and minimize the probability of the odd-mode oscillation, some isolation resistors can be put between the gates pads and between the drains pads [17].

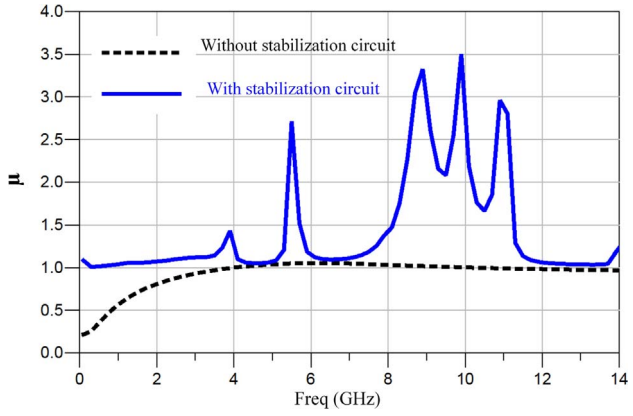


Fig. 9. The stability factor of the proposed PA with and without using the stabilization circuit.

Indeed large gate periphery devices are made of multiple parallel transistors. In these kind of devices, in order to achieve the best performance, all parallel transistors should be loaded uniformly. Otherwise, the PA performance can be degraded [19,34]. E.g. a TGF2023-2–10 transistor consists of eight TGF2023-2-1s. As already shown in Fig. 10, the input and output matching networks are usually connected to the large gate periphery transistor through several wire bonds. Therefore, the impedance seen from the gate or drain of each parallel transistor can be different than that of the neighboring transistors. Just to quantify this effect, the impedances seen by different parallel transistors in a TGF2023-2–10, using the structure in Fig. 10a, are simulated using a 3D full-wave simulator of HFSS and the results are shown in Fig. 10b. As shown in Fig. 10b, each pair of transistors, which are placed at a similar position with respect to the die symmetry line (e.g. transistors 1 and 8), exhibit a similar impedance. But, different pairs of transistors especially the pair 1&8 and pair 4&5 (Fig. 10a) show different impedances. In [34], an altered bond-wire method is presented in which by using longer wire bonds for transistors 1 and 8, the impedance mismatch is compensated. However, this method suffer from two shortcomings; it needs a try and error procedure and the impedance mismatch is not completely compensated.

Often in a hybrid PA, a large number of variables should be optimized. This increases the circuit complexity to a level that the optimum values cannot be obtained manually. Therefore, the circuit performance should be optimized using automated optimization algorithms. The optimization variables include widths, lengths and radiuses of different lines and stubs. The Momentum ADS simulator is used to evaluate the performance of the solutions that are generated by the optimization tool. The optimization goals are the input and output reflection coefficients, power gain, bandwidth and PAE.

2.6. Circuit implementation

The layout and photo of the fabricated sample PA are shown in Fig. 11. The bias network is designed using quarter wave length stubs and bypass capacitors. In addition, a bias circuit is designed in such a way to provide an appropriate sequence for drain and gate voltages applied to the GaN HEMT. This voltage sequence is implemented in our sample PA circuit using a modified version of the bias circuit presented in [35].

An important issue in a PA package design is the cavity resonances. The package box should be designed to grantee that the first mode of the cavity resonance is higher than the maximum frequency at which the PA still provides a power gain. The cavity resonance modes of the designed box for our PA are given in Fig. 12b. The first mode of cavity resonances occurs at 15.36 GHz while the PA has no power gain at

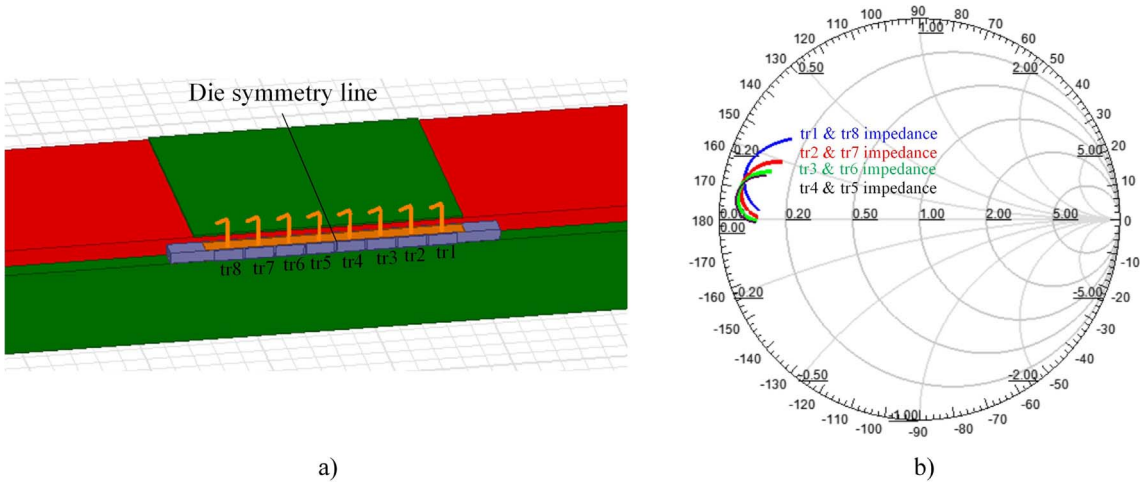


Fig. 10. (a) The 3D model used for calculation of the impedances seen by the parallel transistors in a Tgf2023-2-10 transistor in HFSS simulator. (b) Simulated impedances seen by the parallel transistors.

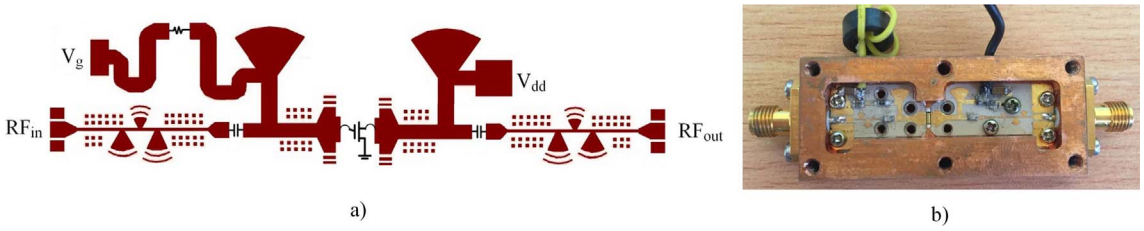
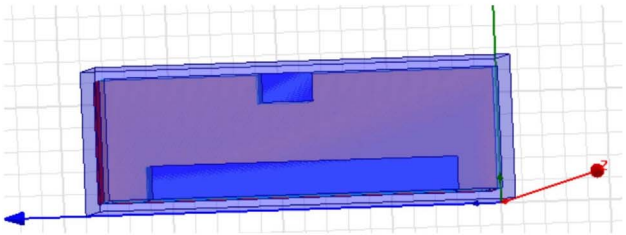


Fig. 11. (a) Layout of the proposed PA circuit. (b) The fabricated proposed PA.



Eigen mode	Frequency (GHz)	Q
Mode1	15.36	3080.98
Mode2	16.259	3115.01
Mode3	18.213	3409.61
Mode4	20.734	3419.15
Mode5	22.035	3818.49

b)

Fig. 12. The cavity resonance simulation of the designed package for the proposed PA circuit. (a) The 3D model used in the HFSS software. The fabricated package box is shown in Fig. 11b. (b) The simulated cavity resonances frequencies of the designed box.

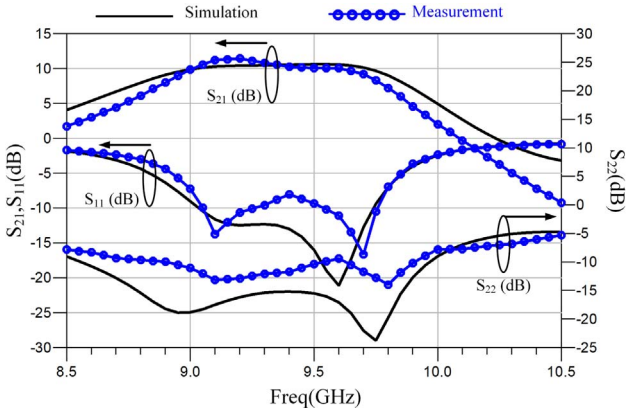


Fig. 13. The simulated and measured small-signal S-parameters of the proposed PA at bias of V_{dd} = 28 and I_d = 500 mA in CW mode.

frequencies higher than 10.5 GHz. In order to tune the RF characteristics of the fabricated PA, some tuning array pads are placed along the matching networks, which can be used for further adjustment of the PA's frequency response after fabrication.

3. Simulation and measurement results of the fabricated sample circuit

As already mentioned, in order to have a fast and reliable design, all the passive elements are first simulated using a 2.5D simulator such as Momentum of ADS software and then the optimized results are checked by a full-wave 3D simulator like HFSS. Furthermore, an accurate nonlinear model of the power transistor, which is provide by Modelithics Inc.[23], is used for large-signal analyses of the circuit. The simulated and measured small-signal S-parameters of the proposed PA at bias of V_{dd} = 28 and I_d = 500 mA in CW mode are shown in Fig. 13. Both of simulated and measured results show a reasonable consistency with each other. As it is shown, an average small-signal S_{21} of 10.5 dB in the frequency range of 9–9.4 GHz is obtained. The input and output

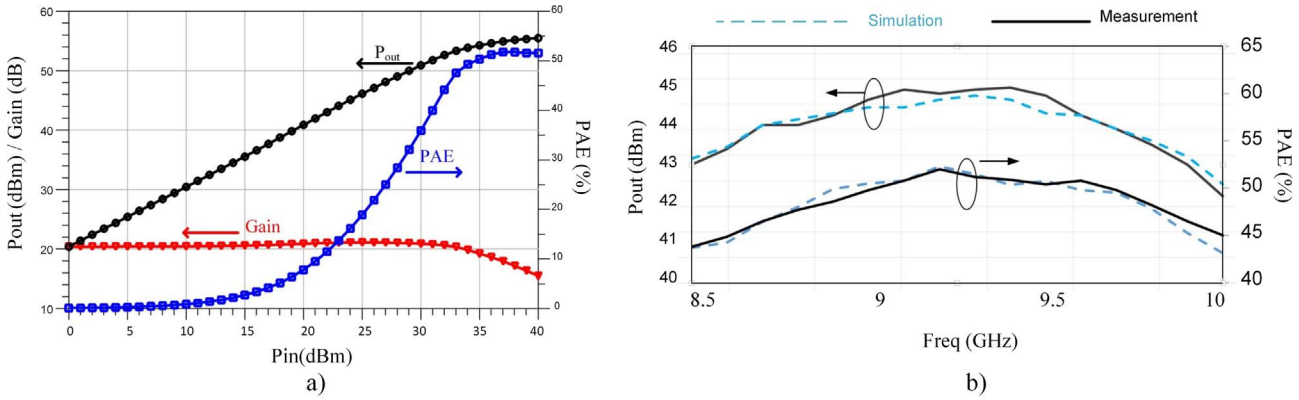


Fig. 14. (a) The measured output power, PAE and power gain of the fabricated proposed PA at frequency of 9.2 GHz. (b) The large signal simulation and measurement results of the proposed PA versus frequency at Pin of 36 dBm.

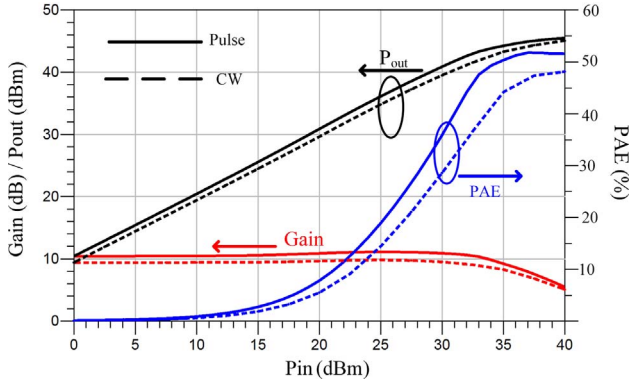


Fig. 15. The measured output power, PAE, and power gain of the proposed PA in CW and pulse modes conditions at frequency of 9.2 GHz.

reflection coefficients are below −8 dB and −12 dB over the desired frequency band, respectively.

The stability simulation results of the proposed PA is shown in Fig. 9. Obviously the PA is unconditionally stable over all frequencies. The simulated and measured output power and PAE are shown in Fig. 14a. The circuit provides an output power of 44.8 dBm and a PAE of 52% at the frequency of 9.2 GHz. As it is shown in Fig. 14b, the minimum measured PAE and minimum P_{out} at the desired frequency band are more than 50% and 44.6 dBm, respectively. These investigations are performed under a pulse mode condition with a duty cycle of 10% and a pulse duration of 20 μs when it was derived using a 5 W GaN HEMT power amplifier.

Thermal effects and consequently the PA operation mode have a great impact on the HPA performance that should be carefully studied. Therefore, the PA characteristics are measured under CW and pulse modes conditions (with a duty cycle of 10% and a pulse repetition frequency (PRF) of 10 kHz). The results in Fig. 15 confirm that the pulsed PA exhibits a higher output power, a better PAE and a higher power gain due to the reduced self-heating effects.

The transistor drain and gate waveforms are shown in Fig. 16 as Pin sweeps from 25 dBm to 36 dBm. By increasing the input power, the input and output capacitors enter into their nonlinear regions. These effects can be used to shape the gate and drain voltage waveforms of the transistor and enhance the PAE of the PA [21,22].

Finally, Table 2 summarizes the performances of the fabricated sample PA and some recently reported high power hybrid PAs in X-band frequencies. Obviously, our systematically fabricated PA exhibits a superior performance as provides a better PAE, a higher gain and a similar frequency bandwidth in comparison with the previously published works.

4. Conclusion

A design methodology for realization of a hybrid high frequency PA is systematically described and a sample 9–9.8 GHz hybrid PA is designed and fabricated using a GaN on SiC HEMT in accordance with proposed method. Also, it is explained how a thermal model of the power transistor, which is obtained using ANSYS software and calibrated by the measured data, can be used for prediction of the device median lifetime. The procedures for stability analysis, unbalance feeding effects and layout optimization are well discussed. In addition,

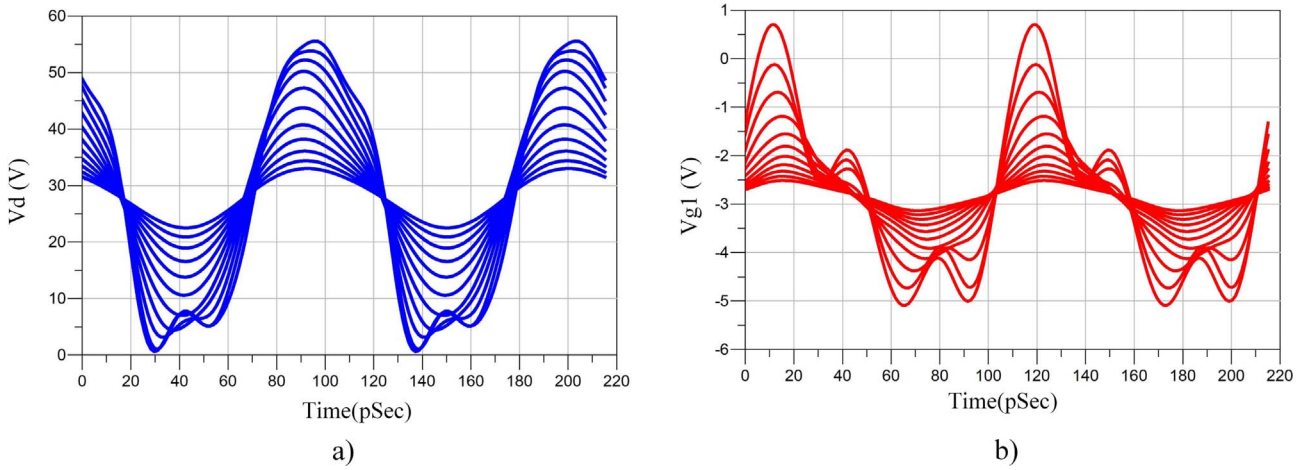


Fig. 16. The transistor waveforms when P_{in} sweeps from 25 dBm to 36 dBm, (a) drain waveform, (b) gate waveform.

Table 2
Summary of the fabricated sample PA performance and its comparison with some previously published designs.

Ref.	Technology	BW (GHz)	P_{out} (W)	Max S_{21} (dB)	PAE_{max} (%)	Area (mm^2)	Substrate
[15]	Hybrid GaN HEMT	9–10	46	8.7	30	15 * 17.8	Alumina (ϵ_r = 9.8, H = 5 mil)
[36]	Hybrid GaN HEMT	8.9–9.9	64	10	45	9.8 * 8.6	PCB (ϵ_r = 40, H = 10 mil)
[37]	Hybrid GaN HEMT	9.5–10.5	10.7	7.5	50	Not reported	PCB (ϵ_r = 38)
[38]	Hybrid GaN HEMT	9.5–10.5	60	10.3	35	21 * 12.9	PCB (ϵ_r = 40 and 9.8 combined)
This work	Hybrid GaN HEMT	9–9.8	30	12	52	8.9 * 30.1	PCB (ϵ_r = 11, H = 10 mil)

it is explained how accurate modeling of the matching networks and wire bonds can influence the PA RF characteristics.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.aeue.2017.12.011.

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