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RESEARCH ARTICLE

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Efficiency enhancement by employing the transistor nonlinear capacitors effects in a 6W hybrid X-band Class-J power amplifier

Mehdi Forouzanfar | **Mojtaba Joodaki**

Electrical Engineering Department, Ferdowsi University of Mashhad, Mashhad, Iran

Correspondence
Mojtaba Joodaki, Electrical Engineering Department, Ferdowsi University of Mashhad, Mashhad, Iran.
Email: joodaki@um.ac.ir

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Abstract

This article presents the design and fabrication of a 6 W X-band hybrid Class-J power amplifier (PA) based on a bare die GaN on SiC HEMT by accurate implementing the transistor nonlinear capacitor effects. The transistor input capacitor is precisely modelled and its nonlinearity effects on Class-J performance is studied for the first time. It is shown that the harmonic generation property of the nonlinear input capacitor, especially at the second harmonic, can be of benefit to shape the transistor gate voltage as a quasi-half wave sinusoidal waveform and consequently, it can improve the power added efficiency (PAE). A complete 3D thermal model of the power transistor is developed using ANSYS software and it is calibrated based on the thermal measured data. The PA achieves 13 dB average power gain over the frequency range of 8.8-9.6 GHz. The drain efficiency and PAE are about 67% and 58% at 9.2 GHz, respectively.

KEYWORDS

Class-J, hybrid, GaN HEMT, power amplifier, X-band

1 | INTRODUCTION

Power amplifier (PA) is one of the most important blocks in high frequency transceivers. Some possible applications of high frequency PAs include mobile communications, wireless systems, pulse radar and medical microwave imaging systems.[1,2]

GaN on SiC HEMTs provide some unique features such as small size, sufficient output power, appropriate thermal performance, small parasitic elements, high power density and good reliability.[3] Therefore, they are an appropriate candidate for realizing high frequency PAs.[4] Different technologies have been used for the integration of high frequency transistors.[2–10] The monolithic microwave integrated circuits (MMICs) provide reliable design, occupy small chip area and thus, exhibit small parasitic elements,[5] but they are not suitable for high power applications and they require a sophisticated fabrication process. The quasi-monolithic integrated circuits have been already implemented in Refs. [6,7], which provide an appropriate frequency response as well as a good thermal characteristic. However, they need thin-film technology for realization.

Hybrid approach is another popular integration method, which can be a convenient choice for implementation of high PAs due to its proper thermal performance.[8,9] Furthermore, it can be realized using inexpensive substrate whereas it does not necessitate any sophisticated manufacturing technology. RF hybrid PAs can be implemented using discrete elements with different substrate materials but they do not provide an appropriate frequency response at few tens of GHz due to the large parasitic elements of the interconnects.[10] Several X-band hybrid PAs have been reported in the literature.[11–16] They provide high output powers, proper thermal behaviours and good power added efficiency (PAE), but they usually show lower bandwidths in comparison with MMIC PAs.[17]

PA must meet several stringent requirements such as wideband frequency response, sufficient gain, adequate drain

efficiency and appropriate linearity performance. Employing the efficiency enhancement methods, which can effectively reduce the transistor power dissipation and thus, increase the reliability and median lifetime of the device, is essential for high power applications. Several topologies have been proposed for realization of high efficiency PAs.[18–32] Reduced conduction angle PAs[18] such as Class-C PA, can provide high efficiency but they do not have sufficient output power and suffer from nonlinearity problems.

The switching PAs such as Class-E and Class-D are well known for their ability to increase the efficiency; however, they cannot easily be realized at X-band frequencies.[19,20] In harmonic tuned PAs,[21–31] accurate shaping of the transistor drain voltage and drain current minimize the dissipated power in transistor. In Class-F PA designs, using a large number of harmonics, the drain voltage and drain current are shaped as a square and half-wave sinusoidal waveforms, respectively.[21] In the inverse Class-F PA, the drain voltage is formed as a half-wave sinusoidal waveform whereas the drain current has a square waveform. Class-F and inverse Class-F PAs provide high efficiencies, but they usually suffer from limited bandwidths.[22] In addition, the realization of matching networks at the third harmonic and higher harmonics is not practically possible at higher frequencies.[23]

A Class-J PA was recently presented in Ref. [24], which theoretically provides a linearity performance and a PAE similar to those of a Class-AB PA,[25] by assuming a linear transistor behaviour. However, in practice, a Class-J PA shows a higher PAE than Class-AB PA due to the harmonic generation property of the transistor nonlinear output capacitor.[26] In addition, it has a broader bandwidth characteristic due to the absence of the short circuit or open circuit matching at the harmonic frequencies. In Class-J PA, drain voltage and drain current are shaped as quasi-half sinusoidal wave with a phase overlap of 45 degrees. This is achieved by a complex fundamental termination and the capacitive second harmonic matching.[24] Another advantage of the Class-J design is its capability to be combined with other classes of designs. For instance, a continuous mode Class-B/J PA was presented in Ref. [25] which gave a wideband characteristic, an adequate PAE and an acceptable linearity performance.

Several design approaches for realization of hybrid Class-J PA have been introduced in Ref. [27–31], which provide appropriate strategies for selecting optimum input/output matching networks at different harmonic frequencies. In order to design an X-band Class-J PA, the second harmonic matching network should be realized at frequencies higher than 16 GHz. Large parasitics of the power transistor and the bond wires in this frequency range can deteriorate the RF frequency response and thus, X-band hybrid Class-J PA cannot easily be realized. However, realization of MMIC X-band Class-J PA is more straightforward due to the absence of interconnects parasitics and extremely accurate and reproducible fabrication process.[17] A low power X-band MMIC Class-J PAs is presented in Ref. [17], which provides a high drain efficiency, a wide band characteristic and a moderate power gain.

Although a schematic design for a hybrid X-band Class-J PA is given in Ref. [32] to briefly investigate some considerations including the third harmonic control and the load harmonic filtering, the results are not so attractive and no measurement and EM simulations, usually required for a reliable high frequency PA design, are presented. We have given a preliminary report on a hybrid X-band Class-J PA in Ref. [15], however the design details, proper characterizations, the theory and reasons behind the improvement are missing.

In the present work, to enable the realization of a hybrid high PAE X-band Class-J PA, in addition to the output capacitor design, the transistor input capacitor is also precisely characterized and modelled and its influence on the PA performance is analysed. By employing this precise model, the harmonic generation property of the nonlinear input capacitor, especially at the second harmonic, is used to change the gate voltage into a quasi-half wave sinusoidal waveform and thus improve the PA PAE. A thermal model of the high power GaN on SiC HEMT is also constructed using ANSYS software and it is calibrated based on measured data. This model predicts the channel temperature under different circumstances, which is very helpful to improve the device median-life time and reliability. Measurement results reveal that the proposed PA provides a good PAE, a sufficient output power and a good thermal performance. In addition, it provides a higher PAE than a Class-AB PA that is realized under similar conditions.

This article is organized in 6 sections. The RF power transistor is characterized in section 2. Section 3 describes principles of the Class-J PA design. The proposed Class-J X-band hybrid PA is described in section 4. Then the simulated and measured results are presented in section 5. Finally, section 6 sums up the important results and concludes the article.

2 | CHARACTERIZATION OF THE GaN HEMT TRANSISTOR

The proposed PA is implemented using a 0.25 μm bare die GaN on SiC HEMT with a maximum output power of 6 W. It provides a high-power density (5 W per mm gate width), an adequate power gain and a good reliability. Therefore, it is well suited for realization of X-band PAs. The I–V curve of the transistor is shown in Figure 1. It is simulated in pulse mode condition with 10% duty cycle and a pulse repetition frequency (PRF) of 10 kHz. Pinch-off voltage, knee voltage and maximum drain current of the transistor are about −3 V,

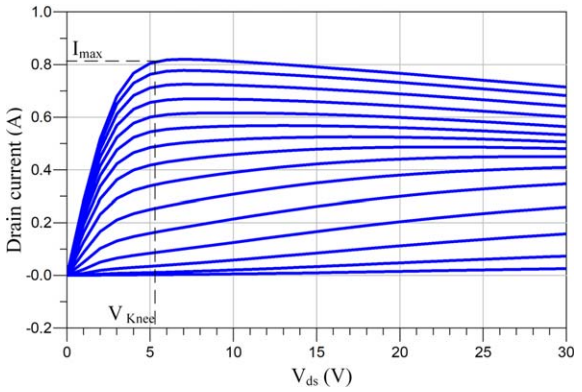

FIGURE 1 Simulated I–V curve of the GaN on SiC HEMT in pulse mode condition with duty cycle of 10% and PRF of 10 kHz

5 V and 820 mA, respectively. Small signal *S*-parameters of the transistor are measured under bias condition of $V_{dd} = 28$ V and $I_d = 120$ mA. As shown in Figure 2, the transistor maximum available gain (MAG) at X-band is higher than 15 dB whereas it is unconditionally stable from 5 GHz to 11 GHz.

The simplified transistor model is shown in Figure 3. This model is derived from the conventional π model of the transistor, in which the C_{gd} capacitor is substituted by its Miller's effects in the input and output. This means that C_{in} is equal to C_{gs} plus the input Miller's effect of C_{gd} and C_{out} is equal to C_{ds} plus the output Miller's effect of C_{gd}. In order to have a reliable hybrid Class-J PA design, parasitic elements of the transistor including drain-source resistor R_{ds}, output capacitor C_{out} and input capacitor C_{in} should be precisely characterized. The influence of a nonlinear output resistance on Class-J PA performance has been already analysed and presented in Ref. [33]. Although it is shown that a nonlinear output resistance can limit the bandwidth of the Class-J PA and should be considered for wideband designs, at X-band frequencies, the output capacitor is the dominant output parasitic element of the transistor and the nonlinear resistor effect can be neglected.

The nonlinear output capacitor of GaN HEMT, shown in Figure 4, can be calculated by accurate transistor *S*-parameters

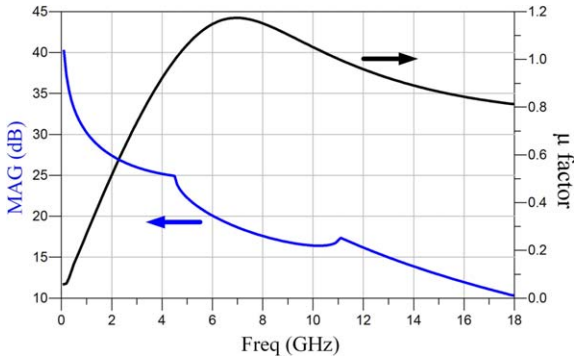

FIGURE 2 Maximum available gain and stability factor of the transistor under bias conditions of $V_{dd} = 28$ V and $I_d = 120$ mA

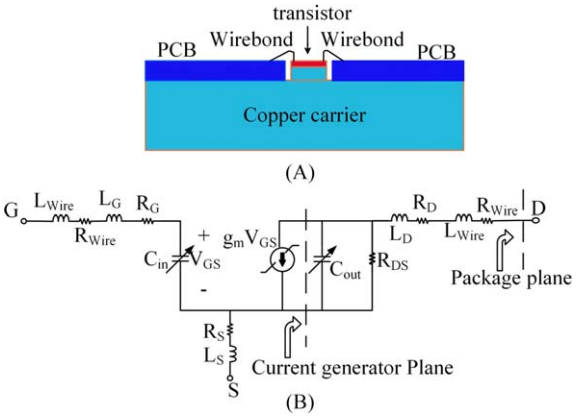

FIGURE 3 (A), Cross section of the transistor attachment. (B), Simplified model of the transistor

measurement and de-embedding the wire bond and pad parasitic effects. C_{out} represents the output capacitor of the transistor including drain-source capacitor C_{ds} and drain-gate capacitor C_{dg}. This capacitor shows a nonlinear characteristic especially when $V_{ds} < V_{knee}$ and it can be well approximated by:

$$C_{out} = 0.448 + 0.45(1 + \tan h(-0.48V_{ds} - 0.081))(\text{pF}) \quad (1)$$

The voltage across the output capacitor for linear and nonlinear capacitors is shown in Figure 5. By increasing the output voltage swing, the capacitor enters into its nonlinear region, and consequently different harmonic frequencies will be generated in the output voltage. This distorted output voltage can improve the PA PAE as it is described in Ref. [26]. The C_{in} can also be calculated by measuring the transistor *S*-parameters for different gate-source voltages and then de-embed the wire bonds and transistor pads parasitic effects. The nonlinear characteristic of the input capacitor, including gate-source capacitor C_{gs} and drain-gate capacitor C_{dg}, is shown in Figure 6. When PA is driven by a large input power, it shows an extreme nonlinear behaviour especially at deep Class-AB bias condition. An analytical expression of C_{in} is extracted using a curve-fitting algorithm (the dashed line in Figure 6) as follows:

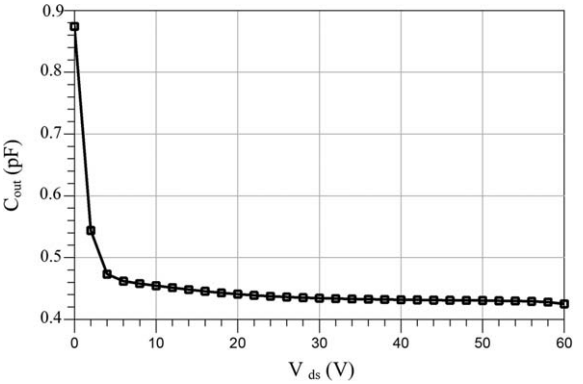

FIGURE 4 Extracted nonlinear output capacitor of the transistor versus drain-source voltage

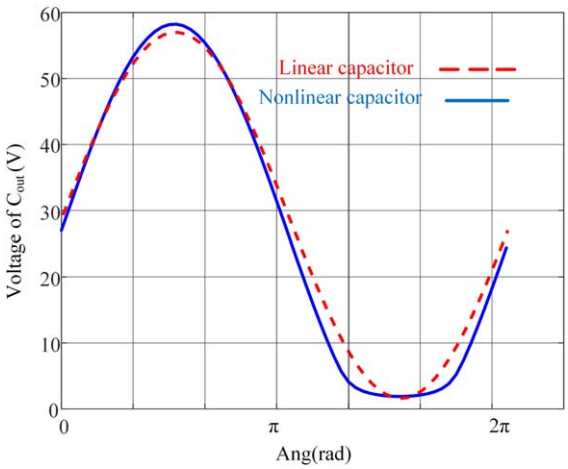

FIGURE 5 Simulated voltage waveforms across the output capacitor with linear and nonlinear capacitors

$$C_{in} = 0.008V_{gs}^4 + 0.025V_{gs}^3 - 0.13V_{gs}^2 + 0.18V_{gs} + 3.65\,(\text{pF}) \tag{2}$$

The gate voltage waveform shaping in the input, which requires appropriate matchings at harmonic frequencies, can affect the PA characteristics.[33] But in an X-band PA, considering the high operating frequency, and relatively large input capacitor of the power GaN HEMT, the matching network at harmonic frequencies cannot easily be realized using the approach performed in Refs. [34–36]. However, the gate voltage can be shaped according to the nonlinear characteristic of the input capacitor as it will be explained in section 5.

A proper thermal management of the power transistor can improve important parameters of PA such as power gain, output power, reliability and median lifetime. Therefore, thermal modelling of the power transistor is vital for high power applications. As shown in Figure 7, a three-dimensional (3D) thermal model of TGF2023-01 GaN on SiC HEMT is constructed using ANSYS software while the temperature dependent thermal properties of all materials are considered.[37] The total drain current of the 10 × 125 μm transistor is about 125 mA. This results in ∼12 mA drain current and 336 mW power dissipation for each drain finger

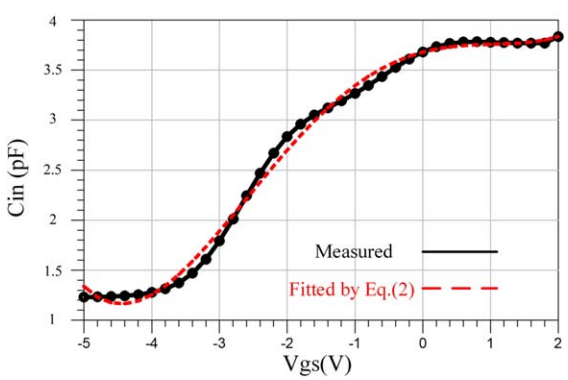

FIGURE 6 Extracted nonlinear characteristic of the input capacitor versus the gate-source voltage

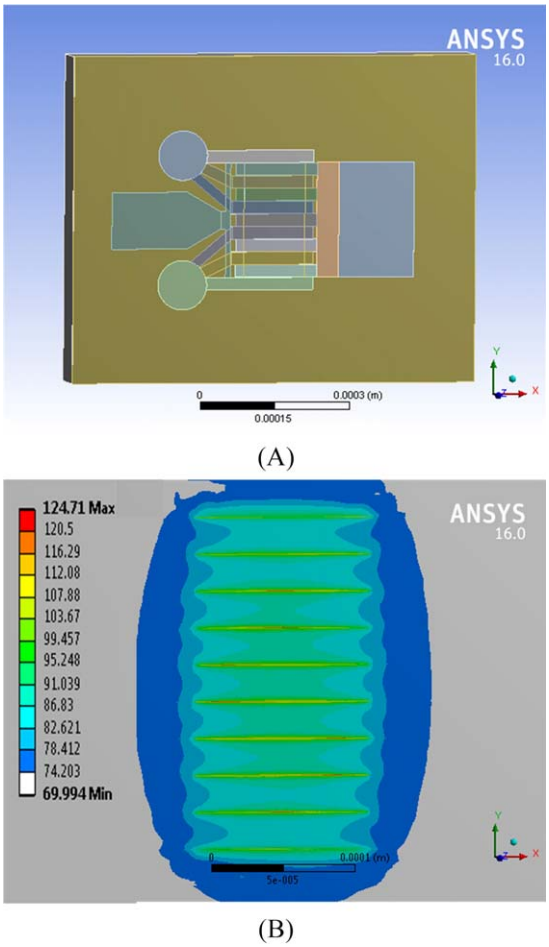

FIGURE 7 (A), Three-dimensional thermal model of the transistor in ANSYS software. (B), The simulated temperature distribution. The maximum channel temperature is reached about 124°C when transistor is biased at V_{dd} = 28 V, I_d = 120 mA in continuous mode with the baseplate temperature of 70°C

at a drain voltage of 28 V. The gate areas are considered as heat sources whereas each gate finger has a power dissipation of 336 mW. As shown in Figure 7, the simulation results show a maximum channel temperature about 124°C with a baseplate temperature of 70°C. According to the simulation results, the calculated thermal resistance of the transistor will be about 16.1°C/W which is in close agreement with the measured thermal resistance of 16°C/W in Ref. [38]. The thermal simulation results of TGF2023-01 are shown in Figure 8. The channel temperature and thermal resistance of the transistor versus its power dissipation are shown in Figure 8A,B. As it is shown, by increasing the transistor power dissipation, the thermal resistance and channel temperature increase too. Figure 8C shows the variation of the channel temperature versus the input power.

The effects of different die attach materials including Sk70N epoxy (with thermal conductivity of 50 W/m °C) and Elcolit 323 silver paste (with thermal conductivity of 3.5 W/m °C) on PA RF performance are investigated using thermal simulations and high frequency measurements. The results

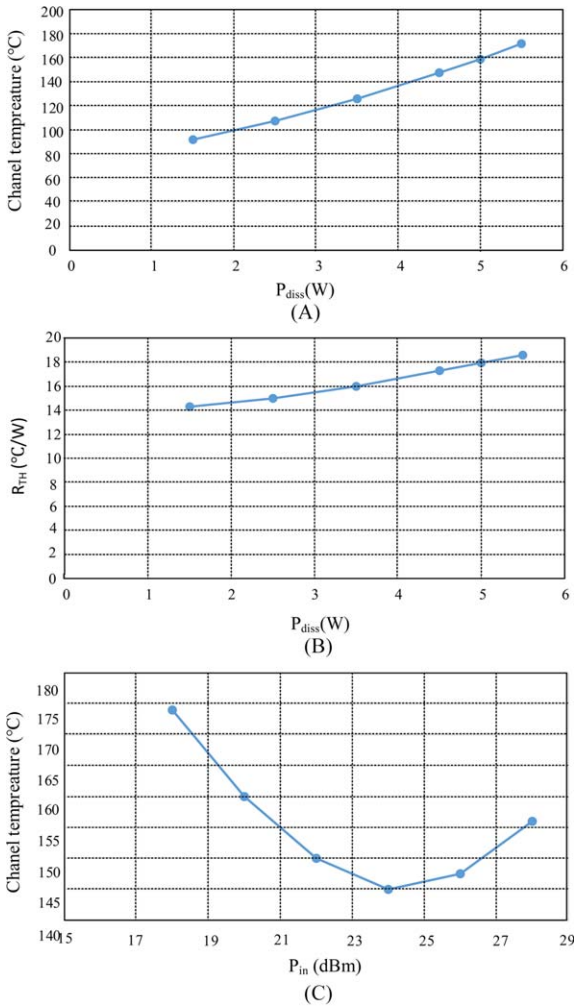

FIGURE 8 The transistor thermal simulation results. (A), The transistor channel temperature versus transistor power dissipation. (B), The transistor thermal resistance versus transistor power dissipation. (C), The transistor channel temperature versus input power

show that a high thermally conductive die attach material can effectively improve the PA's output power and power gain, especially when it works in the continuous mode. Therefore, the power transistor is attached to the carrier with Sk70N epoxy that has a thermal resistance of about 0.9°C/W.

3 | PRINCIPLES OF CLASS-J PA DESIGN

As described in Ref. [26], there is a set of fundamental and second harmonic impedances for Class-AB, Class-J and Class-J* PAs that give the same efficiency and output power for all of them. This design space is given by (3) and (4) as follows[26]:

$$Z_f = R_{opt}(1+\alpha J) \tag{3}$$

$$Z_{2f} = -j\alpha R_{opt} 3\pi/8 \tag{4}$$

In which α is a variable that varies from −1 to 1. α equal to −1, 0 and 1 determines Class-J*, Class-AB and Class-J optimum impedances, respectively. R_{opt} is the optimum fundamental load resistance chosen to achieve the maximum output power. It is given by[26]:

$$R_{opt} = 2\frac{(V_{DD} - V_K)}{I_{max}} \tag{5}$$

The effect of complex fundamental and harmonic impedances on the PA efficiency has already been investigated in Refs. [34–36]. The complex impedance at the fundamental frequency keeps the drain voltage above the knee voltage and prevents the g_m collapse and nonlinear performance.[39] Simplified drain current and drain voltage of a Class-J PA can be expressed as[26]:

$$I(\theta) \approx I_{max}\left(\frac{1}{\pi} + \frac{1}{2}\sin\theta - \frac{2}{3\pi}\cos 2\theta\right) \tag{6}$$

$$V(\theta) = \pi V_{dc}\left(\frac{1}{\pi} - \frac{1}{2}\sin(\theta+\delta) - \frac{2}{3\pi}\cos(2(\theta+\delta))\right) \tag{7}$$

The drain current and drain voltages of ideal Class-J and Class-J* PAs for a linear output capacitor are shown in Figure 9. They have a phase overlap (δ) of about 45 degrees. However, due to the harmonic generation of the nonlinear C_{out}, especially at the second harmonic frequency, the phase overlap between the drain current and the drain voltage can be reduced to obtain a higher efficiency.[26] Several high efficiency PAs have been designed based on the nonlinear output capacitor effects.[40–42] For example, a high efficiency Class-J PA is introduced in Ref. [42] which provides an appropriate PAE by shaping the voltage waveform using a nonlinear C_{out} and employing a resistive fundamental load.

In our design, we have $V_{dd} = 28$ V, $V_{Knee} \approx 5$ V and $I_{max} \approx 0.82$ A. Therefore, according to (3), (4) and (5), the optimum output impedances at the first and the second harmonics are $Z_L = 55 + 55j$ and $Z_{L2} = -65j$, respectively. These calculated impedances are with reference to the current generator plane and should be transferred to the package

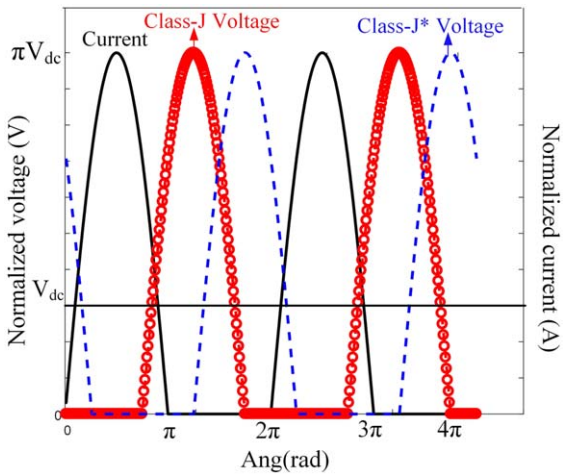

FIGURE 9 Drain current and drain voltage of ideal class-J and class-J* PAs

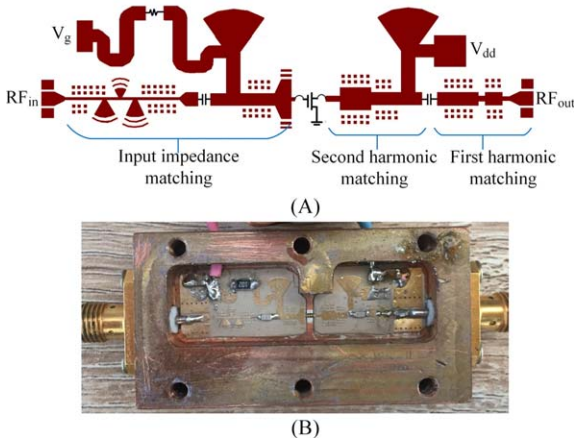

FIGURE 10 (A), Layout of the proposed Class-J PA. (B), The fabricated PA

plane by considering wire bond and pad parasitic elements. The wire bond parasitics (R_{wire}, L_{wire}) are modelled using a high frequency simulator as explained in section 4. The pad parasitics (L_D, R_D) are extracted based on a small signal model which is provided by the manufacturer.[38] Furthermore, the intrinsic parasitic elements (C_{out} and R_{DS}) are calculated by accurate measurements of the transistor *S*-parameters and de-embedding the wire bond and pad parasitics.

4 | THE PROPOSED X-BAND CLASS-J PA

The layout of the proposed Class-J PA is shown in Figure 10. In order to have a reliable design, all passive elements are simulated using Momentum Advance Design System (ADS) and High Frequency Structural Simulator (HFSS) software. The proposed PA is designed based on a commercial nonlinear model of the transistor. The model can be used for both continuous and pulse modes simulations at different bias and thermal conditions while it considers the self-heating effect.

As already mentioned, high power transistors usually exhibit relatively large parasitic elements, which can deteriorate the RF frequency response. Furthermore, in hybrid configuration, the wire bond interconnects exhibit extra parasitic inductances that can limit the PA bandwidth. Therefore, design of wideband hybrid PAs is a challenging work. In the proposed PA, an acceptable bandwidth is achieved by appropriate selection of the substrate, matching network topology and wire bond structure. In order to achieve a wide bandwidth, the discontinuity between the input/output impedance of the transistor and the impedance of bonding pad on the matching network should be minimized.[8] Based on the relatively low input/output impedances of TGF2023-01 transistor at the desired frequency band, a thin substrate with high dielectric constant (Rogers RO3010 with $\varepsilon_r = 11.2$ and $H = 10$ mil) is chosen for the matching networks. This effectively reduces the impedance discontinuities and consequently, improves the PA bandwidth. Rather wideband matchings are achieved using radial stubs and stepped impedance techniques for implementation of the input and output matching networks, respectively.[11,43]

Wire bonds shape has a strong influence on the PA frequency response. Therefore, the wire bonds are precisely modelled using a 3D full-wave high frequency simulator of HFSS. In the proposed PA, 2 parallel 25 μm gold wire bonds with the shortest possible length are bonded on each gate and drain pad (Figure 11A) to reduce the equivalent parasitic impedance of the interconnect structure, and thus increase the bandwidth. The proposed wire bond structure is excited using wave ports in HFSS simulator (Figure 11B) and its high frequency model is extracted up to 20 GHz, which is shown in Figure 11C. L_w, R_w, C_{par} and K are wire bond inductor, wire bond resistor, pad capacitor and coefficient of coupling between the inductors, respectively. In the proposed PA, wire bonds length is about 300 μm while the space between the wire bonds is equal to 60 μm. The extracted L_w, R_w, C_{par} and K are equal to 0.56 nH, 0.2 Ω, 0.05 pF and 0.05, respectively.

The load pull of the transistor at the current generator plane is simulated at the centre of the desired frequency band (9.2 GHz) under a pulse mode condition with duty cycle of 10%. The results show that the maximum P_{out} and maximum PAE are achieved at $Z_{L1} = Z0^*(1.01 + j0.71)$ and $Z_{L1} = Z0^*(0.91 + j0.96)$, respectively while the load impedance at the second harmonic is $Z_{L2} = -60j$ and the source reflection coefficients are $\Gamma_{s1} = 0.62\ e - j172\pi/180$ and $\Gamma_{s2} = 0.74\ e - j125\pi/180$. The simulated load pull shows a good consistency with load pull impedance calculated in the previous section. The

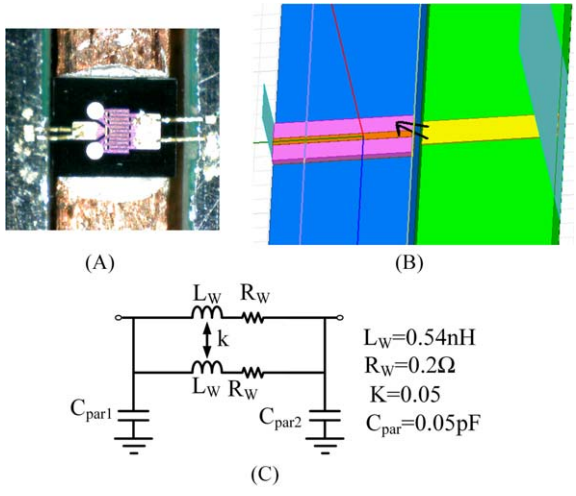

FIGURE 11 The wire bonds: (A), Implementation. (B), Three-dimensional model in HFSS simulator. (C), The simple high frequency model

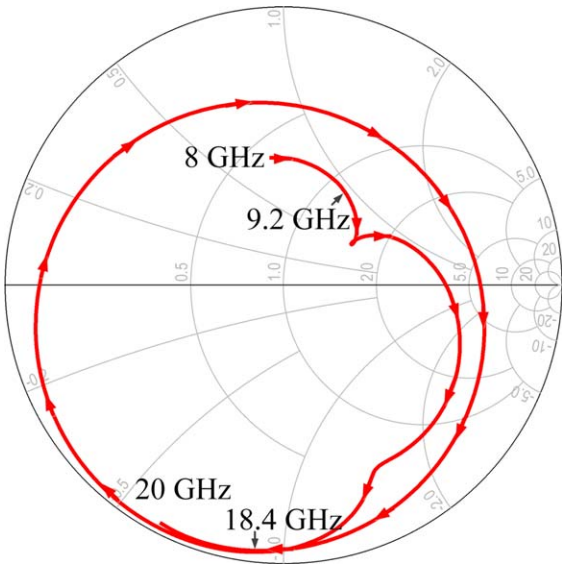

FIGURE 12 The impedance seen from the current generator plane for frequency range of 8 to 20 GHz

impedance, which is seen at the current generator plane is shown in Figure 12 for frequency range of 8 to 20 GHz. As the bias stub-line has a length of λ/4 at the fundamental frequency, it acts as a short circuit at the second harmonic frequency. Therefore, the first part of the matching network is designed for the realization of the second harmonic matching network while the other part is used for the first harmonic matching network (Figure 10A).

Class-J PA design strategy can relax the requirements needed for realization of the output-matching network. Therefore, it can provide a wideband output matching. However, in the case of high power TGF2023-01 transistor, the transistor input impedance is about five times smaller than the transistor output impedance and consequently input matching bandwidth limits the overall bandwidth of PA.

In order to reduce the discontinuity between SMA connectors and the matching network, broadband coaxial-to-microstrip transitions are precisely designed and implemented using CPW structures described in Ref. [44]. The 50Ω microstrip structure has a line width of 200 μm which provides a sufficient power and current handling capability.

The array pads for tuning are placed along the matching networks that can be used to correct the PA frequency response. In order to have an appropriate wire bonding, the PCB copper lines are 3 to 5 μm gold plated. The stability resistor placed in the gate bias network limits the low frequency gain and thus improves the amplifier stability, whereas it does not deteriorate the high frequency performance.

In this circuit, a large number of independent parameters should be optimized. This increases the design complexity, so the optimum values cannot easily be obtained. Therefore, a random optimization tool in ADS software is used to achieve the best performance. The selected optimization variables are: width, length and radius of different microstrip stubs in the circuit. The Momentum simulator in ADS software is used to evaluate the performance of the solutions that are generated by the optimization tool. The optimization goals are: the input and output reflection coefficients, power gain, bandwidth and PAE.

The carrier of transistor is made by gold plated copper, which provides good electrical and thermal resistances. The PA's package should be designed in a way that the first mode of cavity resonance occurs at frequencies where the PA has no gain. All modes of package's cavity resonance frequencies are simulated using Eigen-mode simulation in HFSS software. It is shown that the first mode of package resonance occurs at frequencies higher than 15 GHz where the designed PA has no gain at frequencies higher than 10.5 GHz.

5 | SIMULATION AND MEASUREMENT RESULTS

The measured *S*-parameters that have a reasonable agreement with the corresponding simulated results are shown in Figure 13. An average S_{21} power gain of 13 dB in the frequency range of 8.8–9.6 GHz is obtained. The input and output reflection coefficients are below −7.6 dB and −10 dB over the entire 800 MHz bandwidth, respectively. As shown in Figure 14, the proposed PA is unconditionally stable for all frequencies.

Driving the transistor in the nonlinear region can cause parametric sub-harmonic oscillations due to the nonlinear characteristic of the transistor capacitors.[45] This instability issue strongly depends on the input power level, bias

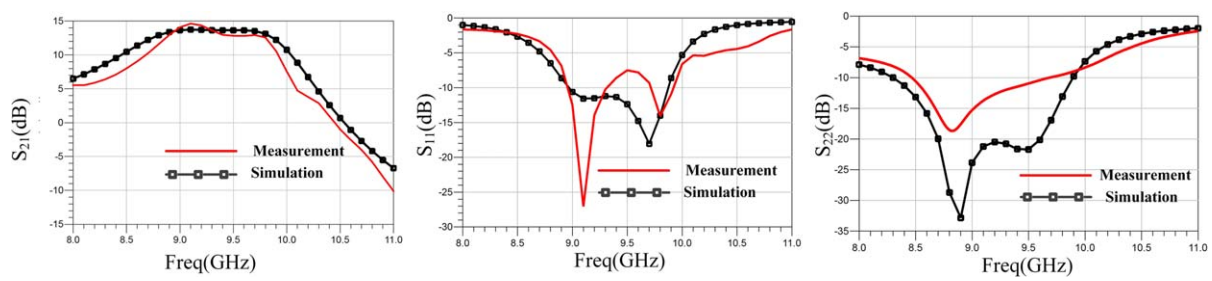

FIGURE 13 Simulated and measured *S*-parameters of the proposed PA with I_d = 120 mA and V_{dd} = 28

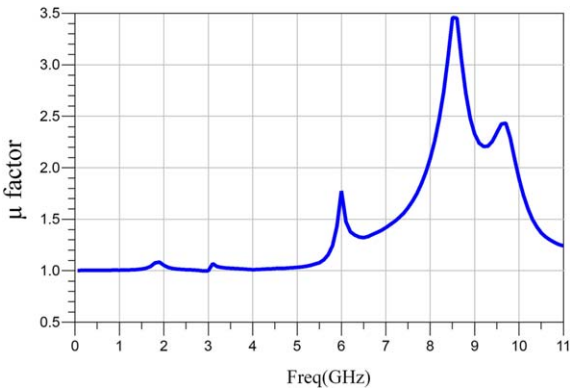

FIGURE 14 Simulated μ factor of the proposed PA at drain bias of 120 mA

condition, operating frequency and load termination.[46] In our PA, the matching networks are designed for a much lower gain at the sub-harmonic frequencies in comparison with that of the fundamental frequency. This suppresses the parametric sub-harmonic oscillations and thus improves the PA stability.

The simulated and measured large signal performance of the proposed PA versus frequency are shown in Figure 15. As shown, it can provide an average output power of 37.6 dBm and average PAE of 57% at the desired frequency band.

As GaN HEMT handles high power densities, thermal effects have great influences on its performance which should be properly considered in the design procedure. Therefore, the power gain, PAE and output power of the proposed PA are measured under 2 different conditions of continuous wave (CW) and pulse mode. The results in Figure 16 confirm that the CW PA exhibits a lower output power, a worse PAE and a smaller power gain, due to its self-heating effects

The transistor drain waveforms are shown in Figure 17A as P_{in} sweeps from 15 dBm to 27 dBm. By increasing the input power, the output capacitor enters into its nonlinear region which results in reducing the phase overlap between the drain current and the drain voltage, and consequently increases the overall PA efficiency. Drain current is shaped based on the second harmonic impedance.[23] It is formed as a

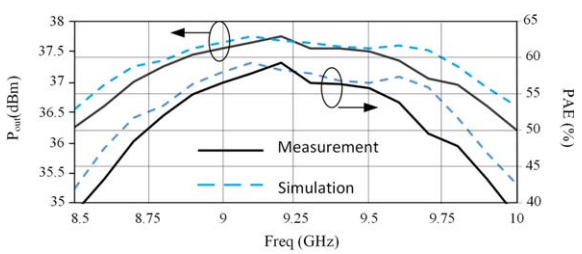

FIGURE 15 The large signal simulated and measured results of the proposed PA versus frequency with P_{in} of 27 dBm

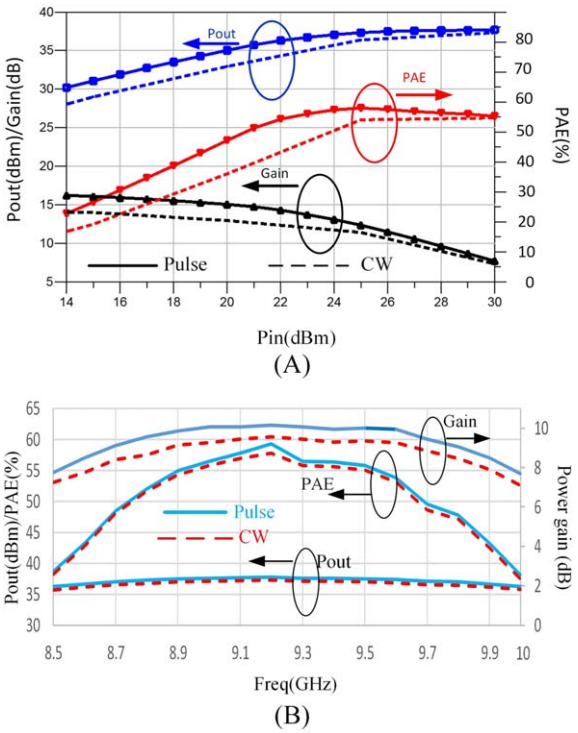

FIGURE 16 (A), Output power, PAE and power gain of the proposed PA in CW and pulse mode conditions at frequency of 9.2 GHz. (B), The P_{out}, power gain and PAE of the proposed PA in CW and pulse mode conditions versus frequency (P_{in} = 27 dBm)

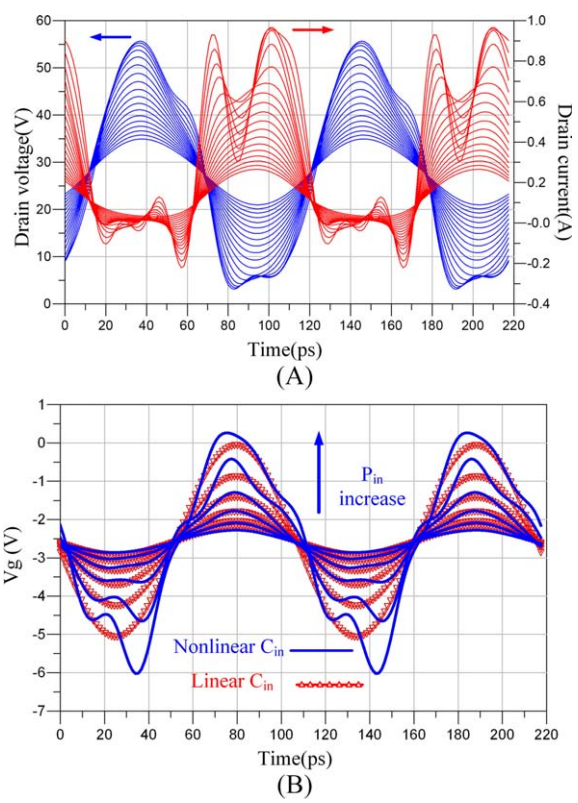

FIGURE 17 (A), Drain voltage and drain current waveforms of the proposed PA versus P_{in} at frequency of 9.2 GHz. (B), The gate voltage waveforms versus P_{in}. P_{in} is swept from 15 dBm to 27 dBm at frequency of 9.2 GHz

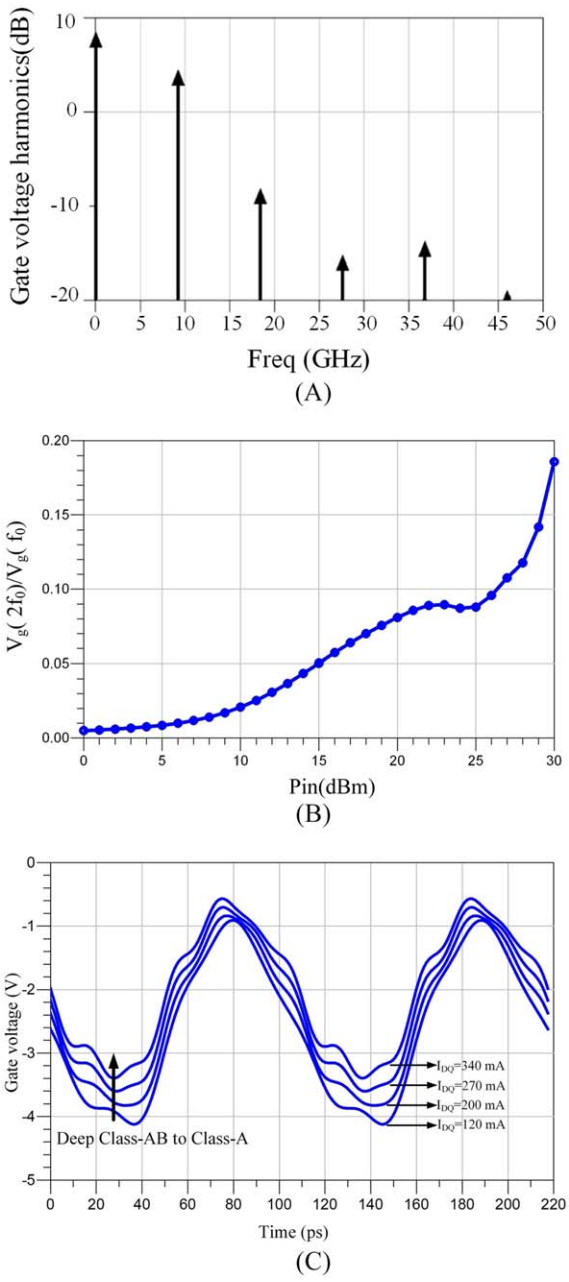

FIGURE 18 (A), The frequency response of the gate voltage at $P_{in} = 27$ dBm. (B), The ratio of the second harmonic to the first harmonic of the gate voltage when P_{in} sweeps from 0 dBm to 30 dBm. (C), The gate voltage waveform when transistor is biased in different deep Class-AB and Class-A conditions. The transistor is driven by a constant P_{in} of 25 dBm at frequency of 9.2 GHz in all cases

bifurcated quasi- rectangular shape for a large input power. This can help to improve PAE of the PA.[42]

Figure 17B shows the transistor gate waveforms for linear and nonlinear input capacitors. In small values of P_{in}, the input capacitor nonlinearity can be neglected and thus the gate voltage can be approximated as a sinusoidal waveform. At higher values of P_{in}, the harmonic generation property of the nonlinear C_{in}, especially at second harmonic, shapes the gate voltage as a quasi-half-wave sinusoidal waveform.

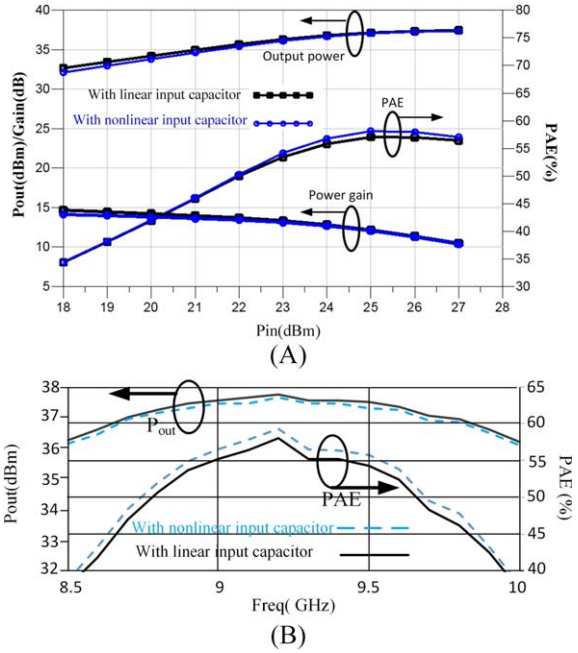

FIGURE 19 The PA output power, power gain and PAE for linear and nonlinear input capacitors: (A), versus P_{in} at frequency of 9.2 GHz and (B), versus frequency with P_{in} of 27 dbm

Based on the extracted input capacitor, deep Class-AB bias condition shows higher input capacitor nonlinearity in comparison with that of the Class-A condition.

The frequency response of the gate voltage at $P_{in} = 27$ dBm, when the transistor is biased in deep Class-AB, is shown in Figure 18A which exhibits a relatively large second harmonic voltage. The voltage ratio of the second harmonic to the first harmonic is shown in Figure 18B. At small values of P_{in}, this ratio is less than 1% while it reaches about 19% at $P_{in} = 30$ dBm. The gate bias influence on the gate voltage waveform is shown in Figure18C, where the transistor is biased in different biases driven by the same input power. As shown, in deep Class-AB condition the input capacitor nonlinearity shapes the gate voltage as a quasi- half-wave sinusoidal waveform and consequently improves the PAE with a small reduction in the maximum output power. Figure 19 shows how the nonlinear input capacitor affects the PA output power and PAE. The PAE improvement by the nonlinear input capacitor is evident.

The test setup of the large signal measurement is shown in Figure 20. The PA is driven using a 2 W GaAs MMIC PA. Two separate Class-J and Class-AB PAs are simultaneously

FIGURE 20 The test setup of the large signal measurement

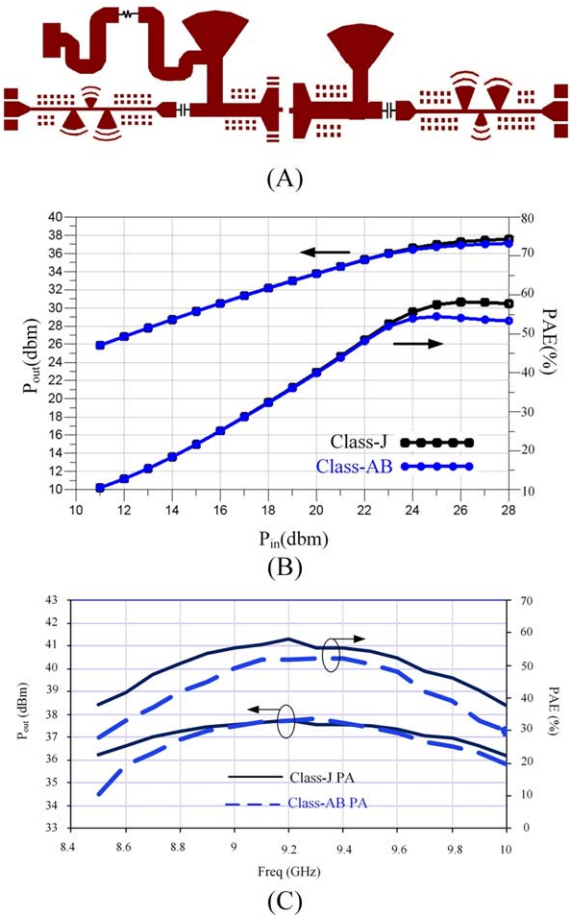

FIGURE 21 (A), The layout of the Class-AB PA. (B), Comparison of the large signal measured results of the Class-J and the Class-AB PAs versus P_{in} at frequency of 9.2 GHz. (C), Comparison of the large signal measured results of the Class-J and the Class-AB PAs versus frequency at P_{in} of 27 dBm

designed and fabricated using the same transistor in order to compare their characteristic in term of PAE and output power. Both of them are biased in pulse mode condition with similar bias point while they use identical die attach material. In Class-AB PA, the fundamental and the second harmonic matching impedances at the current generator plane are equal to R_{opt} and zero, respectively. The designed layout of the Class-AB PA is given in Figure 21A and its large signal measured results are compared with those of the Class-J PA in Figure 21B,C. The measurements are performed with a duty cycle of 10% and a period of 20 μs. An output power of 37.6 dBm with a PAE of 58% and drain efficiency of 67% at 9.2 GHz are achieved for the Class-J PA. The PAE of the proposed PA is about 9% higher than that of the Class-AB PA which is realized in similar conditions.

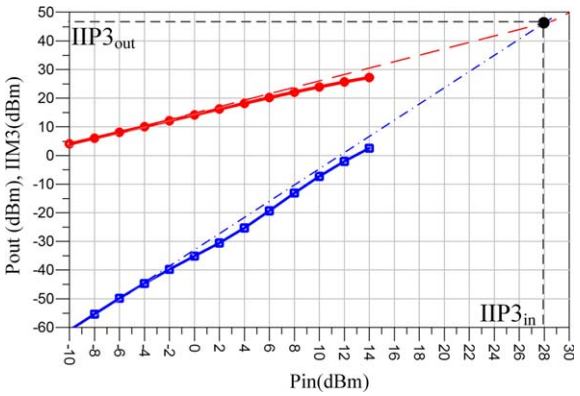

FIGURE 22 Simulated IIP3 of the proposed PA at frequency of 9.2 GHz where a 2-tone test is performed with 100 MHz spacing

IIP3 is an important parameter of linearity evaluation for high PAs so that in the evidence of a small IIP3, strong interferers can exist in the desired frequency band. As shown in Figure 22, the input IIP3 of the proposed PA is about 28 dBm, which is quite acceptable for the PA to be well robust against the near interferences. Simulations are performed using a 2-tone test at 9.2 GHz with a 100 MHz spacing.

TABLE 1 Summary of the proposed PA performance and its comparison with some previously published designs

Ref	PA class	Technology	Freq. (GHz)	P_{out} (dBm)	S_{21max} (dB)	PAE_{max} (%)	Supply voltage (V)
[3]	Class-J	GaN MMIC	2.2–3	27	10	58	12
[2]	Class-J	InGaP/GaAs HBT MMIC	1.7-2	28	35.8	56	3.3
[33]	Class-J	AlGaAs–InGaAs pHEMT MMIC	3.5–7	27.8	13	62	3.8
[17]	Class-J	GaAs pHEMT MMIC	7.5–11.5	28.5	7	65[a]	8
[26]	Class-J	GaN HEMT Hybrid	2.14	40.5	21	77 (8% relative improvement in comparison with Class-AB)	30
This work	Class-J	GaN HEMT Hybrid	8.8–9.6	37.4	14	57 (9% relative improvement in comparison with Class-AB)	28

[a]This is the drain efficiency, its PAE was not reported.

Although, our major aim in this article was constructing a design approach for the implementation of high efficiency hybrid X-band Class-J PA considering the transistor nonlinear input capacitor effects, comparing the work with other recent researches in this field would be very useful. Table 1 summarizes the performances of the proposed PA and some recently reported Class-J PAs. Obviously, this work exhibits superior PAE and an adequate bandwidth. Even in comparison with the 2.4 GHz Hybrid Class-J PA in Ref. [26], it provides a similar relative PAE improvement over a broader bandwidth. GaAs pHEMT MMIC Class-J PA reported in Ref. [17] shows a broader bandwidth, due to MMIC implementation, but gives a much lower output power, a smaller power gain and a bit lower drain efficiency.

6 | CONCLUSION

An 8.8–9.6 GHz Class-J hybrid PA is designed and fabricated based on GaN on SiC HEMT. The proper matching at the second harmonic frequency has been achieved even for a high power GaN on SiC HEMT through accurate modelling of the matching networks and bond wires. Beside the usage of the nonlinear transistor output capacitor, which produces a second harmonic voltage and thus decreases the phase shift between the drain voltage and the drain current waveforms, we show that the nonlinear input capacitor can also help to shape the gate voltage as a quasi-half wave sinusoidal waveform and improve the PA PAE. As a result, the proposed PA exhibits an appropriate PAE, a moderate bandwidth and an acceptable linearity performance. A thermal model of the power transistor is obtained using ANSYS software and calibrated by measured data provided by the transistor manufacturer. In order to have the best performance, different parameters of the circuit are optimized.

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ORCID

Mojtaba Joodaki http://orcid.org/0000-0002-2239-1271

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AUTHOR BIOGRAPHIES

MEHDI FOROUZANFAR was born in Birjand, Iran, in 1984. He received the BS and MS degrees in electrical engineering from Ferdowsi university of Mashhad in 2006 and 2009, respectively. He is currently working toward the PhD degree at Ferdowsi University of Mashhad. His research interests include modelling, design, and analysis of RF microwave circuits.

MOJTABA JOODAKI (S'2001-M'2003-SM'2006) was born in Khorram Abad, Iran in 1970. He received his BS and MSc in electrical and electronic engineering from Iran Science and Technology University in 1994 and Tarbiat Modarres University, Tehran, Iran, in 1997 and his PhD degree in electrical engineering from Kassel University, Kassel, Germany, in 2002, respectively. He joined ATMEL Germany GmbH, Heilbronn, Germany as a device engineer in 2002. There, he was working on technology development, modeling and characterization of Si and SiGe-based devices for RF applications. In April 2005, he joined Infineon Technologies AG in Munich, Germany as a development engineer, where he was responsible for EMI/EMC of memory modules. In his last industrial position, from Oct. 2006 till July 2009, he was a device engineer at Qimonda GmbH, Dresden, Germany, involved in developing nano-transistor for DRAM products. Then, he started working as a visiting scientist and lecturer at the Institute of Nanostructure Technologies and Analytics (INA) at Kassel University, where he defended his Habilitation dissertation in April 2011. Since Sept. 2010, he has been with the Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran, where he was an Assistant Professor and became an Associate Professor in Nov. 2011. His research interests include modeling, characterization and fabrication of passive and active devices (organic and inorganic) for high frequency and optoelectronic applications and electromagnetic compatibility of electronic products. He heads EMI/EMC and Microwave Technology Research Lab at Electrical Engineering Department and Organic Electronics Lab, at Sun-Air Research Institute, both of them at Ferdowsi University of Mashhad, Mashhad, Iran. Mr. Joodaki has been awarded several prizes for his scientific activities, including the best dissertation prize of north Hessen Universities from the Association of German Engineers (VDI) in 2004, Young Graduated Research Fellowship of the GAAS Association in the European Microwave Week 2001 and 2002, and F-Made Scholarship of SPIE 2002. He was also selected as a top researcher of the year 2014 at Ferdowsi University of Mashhad. He is a Life Member of the International Society for Optical Engineering (SPIE).

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